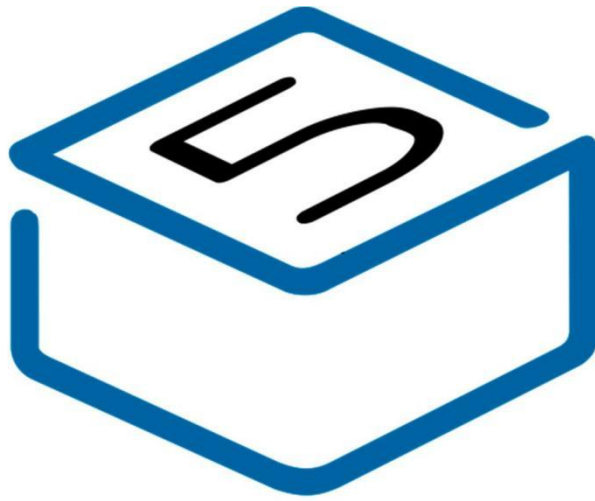


StackChan



M5STACK

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V0.01

Company Name: M5Stack Technology Co.,Ltd
Address: Block A10, Expo Bay South Coast, Fuhai Street, Bao'an District,
Shenzhen,Guangdong,China



TABLE OF CONTENTS

TABLE OF CONTENTS	2
1. OUTLINE	3
1.1 Hardware Composition	3
2. PIN DESCRIPTION	4
2.1. USB INTERFACE	4
2.2. GROVE INTERFACE	4
3. FUNCTIONAL DESCRIPTION	5
3.1. CPU AND MEMORY	5
3.2. STORAGE DESCRIPTION	5
3.2.1. External Flash and SRAM	5
3.3. CPU CLOCK	6
3.4. RTC AND LOWPOWER MANAGEMENT	6
4. ELECTRICAL CHARACTERISTICS	7
4.1. ABSOLUTE MAXIMUM RATINGS	7
4.2. WIFI RADIO AND BASEBAND	7
5. FCC Warning	8



1. OUTLINE

StackChan is ESP32 board which based on ESP32-S3 chip, contained 2-inch TFT screen. The board is made of PC+ABC.



1.1 Hardware Composition

The hardware of CORES3: ESP32-S3 chip, TFT screen, Green LED, Button, GROVE interface, TypeC-to-USB interface, Power Management chip and battery.

ESP32-S3 The ESP32 is a dual-core system with two Harvard Architecture Xtensa LX6 CPUs. All embedded memory, external memory and peripherals are located on the data bus and/or the instruction bus of these CPUs. With some minor exceptions (see below), the address mapping of two CPUs is symmetric, meaning that they use the same addresses to access the same memory. Multiple peripherals in the system can access embedded memory via DMA.

TFT Screen is a 2-inch color screen driven IILI9342C with a resolution of 320 x 240. Operating voltage range is 2.6~3.3V, working temperature range is -25~55°C.

Power Management chip is X-Powers's AXP2101. The operating voltage range is 2.9V~6.3V and the charging current is 1.4A.

StackChan equips ESP32 with everything needed for programming, everything needed for operation and development



2. PIN DESCRIPTION

2.1. USB INTERFACE

M5CAMREA Configuration Type-C type USB interface, support USB2.0 standard communication protocol.



2.2. GROVE INTERFACE

4p spacing 2.0mm M5CAMREA GROVE Ports.A, Port.B, and Port.C, the internal cables are connected to GND, 5V, GPIO1, GPIO2, GPIO8, GPIO9, GPIO17, and GPIO18.



3. FUNCTIONAL DESCRIPTION

This chapter describes the ESP32-S3 various modules and functions.

3.1. CPU AND MEMORY

Xtensa® dual-core 32-bit LX7 microprocessor, up to 240 MHz

- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC
- SPI, Dual SPI, Quad SPI, Octal SPI, QPI and OPI interfaces that allow connection to *multiple flash and external RAM*
- Flash controller with cache is supported
- Flash in-Circuit Programming (ICP) is supported

3.2. STORAGE DESCRIPTION

3.2.1. External Flash and SRAM

ESP32-S3 supports SPI, Dual SPI, Quad SPI, Octal SPI, QPI and OPI interfaces that allow connection to multiple external flash and RAM.

The external flash and RAM can be mapped into the CPU instruction memory space and read-only data memory space. The external RAM can also be mapped into the CPU data memory space. ESP32-S3 supports up to 1GB of external flash and RAM, and hardware encryption/decryption based on XTS-AES to protect users' programs and data in flash and external RAM.

Through high-speed caches, ESP32-S3 can support at a time up to:

- External flash or RAM mapped into 32 MB instruction space as individual blocks of 64 KB
- External RAM mapped into 32 MB data space as individual blocks of 64 KB. 8-bit, 16-bit, 32-bit, and 128-bit reads and writes are supported. External flash can also be mapped into 32 MB data space as individual blocks of 64 KB, but only supporting 8-bit, 16-bit, 32-bit and 128-bit reads.



3.3. CPU CLOCK

The CPU clock has three possible sources:

- External main crystal clock
- Internal fast RC oscillator (typically about 17.5 MHz, and adjustable)
- PLL clock

The application can select the clock source from the three clocks above.

The selected clock source drives the

CPU clock directly, or after division, depending on the application. Once the CPU is reset, the default clock

source would be the external main crystal clock divided by 2.

3.4. RTC AND LOWPOWER MANAGEMENT

With the use of advanced power-management technologies, ESP32-S3 can switch between different power modes. (see table1).

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- Modemsleep mode: The CPU is operational and the clock speed can be reduced. The wireless baseband and radio are disabled, but wireless connection can remain active.
- Lightsleep mode: The CPU is paused. The RTC peripherals, as well as the ULP coprocessor can be woken up periodically by the timer. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip. Wireless connection can remain active. Users can optionally decide what peripherals to shut down/keep on (refer to Figure 1), for power-saving purpose.
- Deepsleep mode: CPU and most peripherals are powered down. Only the RTC memory is powered on and RTC peripherals are optional. Wi-Fi connection data are stored in the RTC memory. The ULP coprocessor is functional.

Current Consumption in LowPower Modes: TABLE 1

Work mode	Description	Typ (μ A)
Light-sleep	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance.	240 ¹
Deep-sleep	RTC memory and RTC peripherals are powered on.	8
	RTC memory is powered on. RTC peripherals are powered off.	7
Power off	CHIP_PU is set to low level. The chip is powered off.	1



4. ELECTRICAL CHARACTERISTICS

4.1. ABSOLUTE MAXIMUM RATINGS

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SPI	Voltage applied to power supply pins per power domain	-0.3	3.6	V
I_{output}^*	Cumulative IO output current	—	1500	mA
T_{STORE}	Storage temperature	-40	150	°C

1. VIO to the power supply pad, Refer ESP32 Technical Specification Appendix IO_MUX, as SD_CLK of Power supply for VDD_SDIO.

4.2. WIFI RADIO AND BASEBAND

The ESP32-S3 Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- 802.11n 0.4 μ s guard-interval
- Data rate up to 150 Mbps
- RX STBC (single spatial stream)
- Adjustable transmitting power
- Antenna diversity:

ESP32-S3 supports antenna diversity with an external RF switch. This switch is controlled by one or more

GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.



4.3. BLUETOOTH LE RF TRANSMITTER (TX) SPECIFICATIONS

Table 3: Transmitter Characteristics Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	-25.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $ f_n _{n=0, 1, 2, \dots, k}$	—	2.50	—	kHz
	Max $ f_0 - f_n $	—	2.00	—	kHz
	Max $ f_n - f_{n-5} $	—	1.39	—	kHz
	$ f_1 - f_0 $	—	0.80	—	kHz
Modulation characteristics	$\Delta f_{1_{avg}}$	—	249.00	—	kHz
	Min $\Delta f_{2_{max}}$ (for at least 99.9% of all $\Delta f_{2_{max}}$)	—	198.00	—	kHz
	$\Delta f_{2_{avg}}/\Delta f_{1_{avg}}$	—	0.86	—	—
In-band spurious emissions	± 2 MHz offset	—	-37.00	—	dBm
	± 3 MHz offset	—	-42.00	—	dBm
	$> \pm 3$ MHz offset	—	-44.00	—	dBm

4.4. BLUETOOTH LE RF RECEIVER (RX) SPECIFICATIONS

Table 4: Receiver Characteristics Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	-97.5	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	9	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-3	—	dB
	F = F0 - 1 MHz	—	-3	—	dB
	F = F0 + 2 MHz	—	-28	—	dB
	F = F0 - 2 MHz	—	-30	—	dB
	F = F0 + 3 MHz	—	-31	—	dB
	F = F0 - 3 MHz	—	-33	—	dB

5. FCC Warning

FCC Caution:

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:



Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does -cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement: This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

